

Fig. 1

FIG. 2 is a diagram illustrating a time slot structure for a 9-bit data bus. The diagram shows a sequence of time slots (Time slot 0, Time slot 1, Time slot 2, Time slot 3) and a corresponding 9-bit data bus. The data bus is divided into four segments, each containing 9 bits. The segments are labeled 210, 212, 214, and 216. The data transfer occurs when the second FAS is found (212). The incoming time slot is aligned to the internal bus (216).

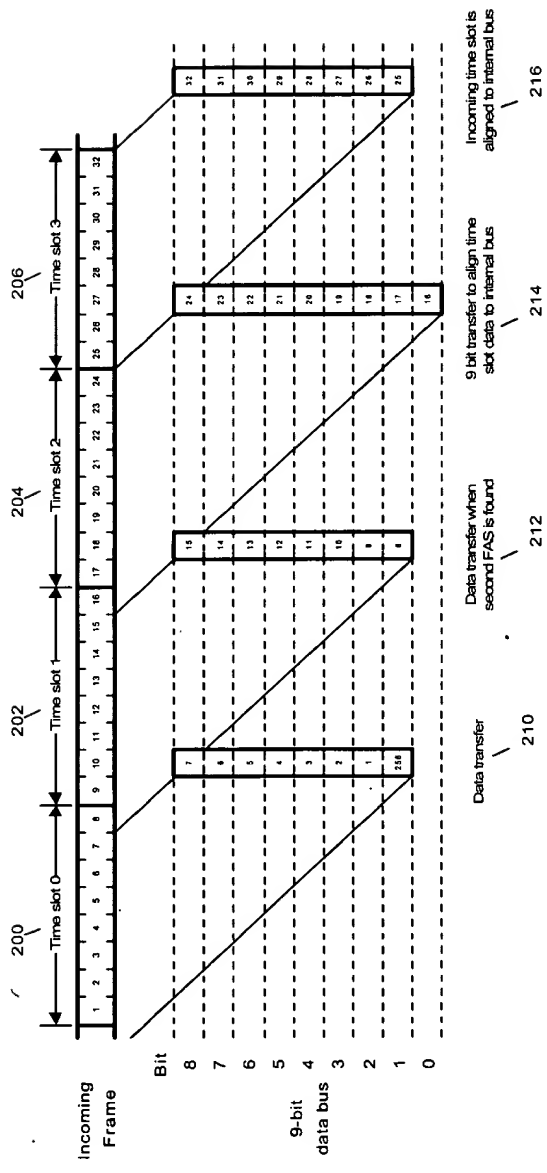


FIG. 2

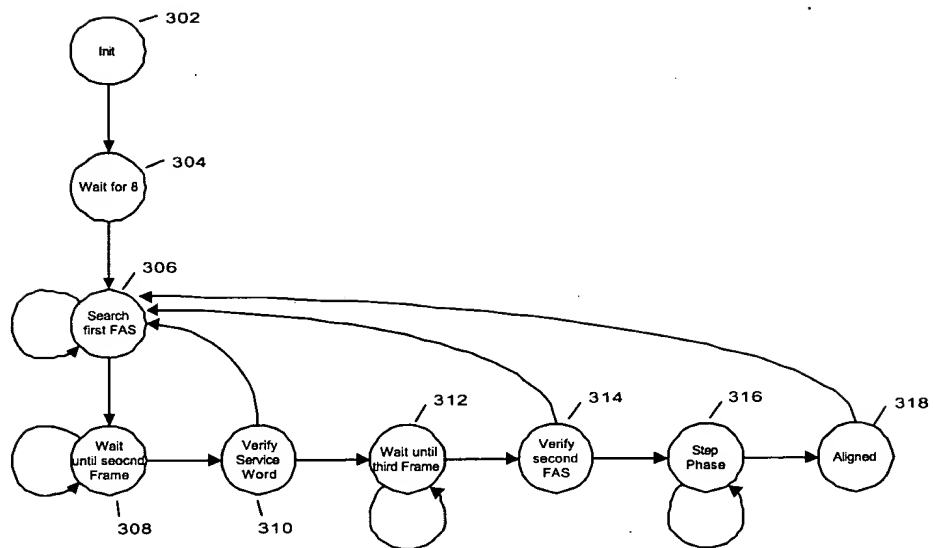


Figure 3